Department of Electronics
Faculty of Engineering, Carleton University,
Ottawa, Canada.

ELEC 2607 [0.5 credit]
Switching Circuits

Course Description

Digital systems, binary numbers, Boolean algebra, logic gates, gate-level minimization, combinatorial circuits, logic circuit modeling and simulation, programmable Logic devices. Flip-flops, latches, sequential circuits, state graphs and state minimization. Counters, registers, and memory. Hazards. Asynchronous sequential circuits, race free assignment, realization.

Includes: Experiential Learning Activity
Precludes additional credit for SYSC 2310.
Prerequisite(s): PHYS 1004 or PHYS 1002 and second-year status in Engineering.
Lectures three hours a week, laboratory three hours alternate weeks.

Specific Goals - Student Learning Objectives

Upon completing this course, students will achieve the following learning objectives:

1. *Hands-On Experimentation and Documentation:*
   - Conduct experiments to grasp the intricacies of logic design and prototyping, cultivating essential hands-on skills.
   - Effectively communicate experiment results through well-structured and appropriately formatted written reports.
2. *Number Systems, Boolean Algebra, and Application:*
   - Proficiently convert between different number systems and harness the power of Boolean algebra.
   - Recognize the practical applications of these concepts in modern digital systems.
3. *Logic Gates, Combinational Circuit Design, and Optimization:*
   - Develop a strong foundation in logic gates and their applications in designing combinational circuits.
   - Optimize designs for resource efficiency, delving into real-world examples that highlight the significance of minimal product-of-sums or sum-of-products forms.
4. *Sequential Logic and Finite State Machines:*
   - Understand sequential logic components' roles in memory units and control systems.
   - Master the art of designing and analyzing finite state machines, integral to modern digital control and communication.
5. *Datapath Components:*
   - Explain the purpose of essential datapath components, such as Registers, Adders, Shifters, Comparators, Counters, Multipliers, Arithmetic-Logic Units (ALUs), and RAM.
   - Identify their collective role in achieving complex digital system functionalities.
6. *Hardware Description Languages (HDLs) and RTL Design:*
   - Design register-transfer level (RTL) circuits using a high-level hardware description language (VHDL or Verilog).
   - Comprehend the pivotal role of HDLs in bridging abstract designs with concrete digital implementations.
7. *Modeling, Synthesis, and Industry Relevance:*
   - Recognize the shift towards modeling and synthesis-based design in modern billion-transistor digital systems.
   - Appreciate the practical relevance of these skills in shaping the digital landscape.
8. *State-of-the-Art Methodologies and Future Trends:*
   - Familiarize yourself with the latest state-of-the-art methodologies, techniques, and paradigms in logic circuit design.
   - Stay updated with industry trends and advancements to ensure your skills remain aligned with contemporary design challenges.

By the end of this course, you will possess a comprehensive toolkit encompassing theoretical knowledge, practical skills, and an understanding of modern trends, positioning you to excel in the dynamic field of logic circuit design.

Resources

- Course Brightspace site
- Primary text
    - M Morris Mano, Michael D. Ciletti. "*Digital design: with an introduction to the Verilog HDL, VHDL, and system Verilog*." (2017).
      ISBN-10: 9780134549897 | ISBN-13: 978-0134549897
- Additional resources
    - John F. Wakerly, "*Digital Design: Principles and Practices*", 5/E, (2018)
      ISBN-10: 013446009X | ISBN-13: 9780134460093.
    - Victor P. Nelson, Bill D. Carroll, H Troy Nagle, David Irwin, "*Digital Logic Circuit Analysis and Design*", 2/E (2020)

Evaluation Methods

The course grade will be evaluated as follows:

Method of Evaluation	% of Final Grade	Due Dates*
Lab Assignments (Individual)	25	lab days
Midterm Exam (Individual)	30	After week 6
Final Exam (Individual)	45	TBA

Notes:

- The exams are for evaluation purposes only and will not be returned to the student.
- Health and Safety: See https://carleton.ca/ehs/programs/working-lab/laboratory-health-and-safety/ for general guidelines.

Satisfactory term work

- In order to pass the course students must achieve satisfactory performance during the term.
- Satisfactory performance during the term requires completion of all lab experiments with a combined average grade of >40% on lab reports.
- The final exam must be completed with a minimum grade of 40% to pass the course.

Instructor information

- Name: Arash Ahmadi
- Office: Mackenzie Building 5146
- Office Hours: by email appointment
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Graduate Assistant (GA) information (TBA)

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4	Nadia Ahmed	nadianahmed@cmail.carleton.ca	**TBA**

Class and lab information

- Class Location: **ME 3275** (Mackenzie Building)
- Class Time: **10:05 AM - 11:25 PM Tuesday and Thursday**
- Lab Time: refer to your schedule.
- Pre-requisites, from the current Carleton University Undergraduate Calendars (https://calendar.carleton.ca/undergrad/courses/ELEC/).

Course Schedule

Please note the following course schedule is approximate.

Week	Date	Subject/Activity	Textbook Chapter or Readings
1	Sep. 5	Digital Systems and Binary Numbers	Chapter 1
2	Sep. 10	Digital Systems and Binary Numbers	Chapter 1
	Sep. 12	Boolean Algebra and Logic Gates	Chapter 2
3	Sep. 17	Boolean Algebra and Logic Gates	Chapter 2
	Sep. 19	Gate-Level Minimization	Chapter 3
4	Sep. 24	Gate-Level Minimization	Chapter 3
	Sep. 26	Gate-Level Minimization	Chapter 3
5	Oct. 1	Combinational Logic	Chapter 4
	Oct. 3	Combinational Logic + Hardware Description Languages (HDL)	Chapter 4
6	Oct. 8	Combinational Logic + HDL	Chapter 4
	Oct. 10	Combinational Logic + HDL	Chapter 4
7	Oct. 15	Combinational/Synchronous Logic	Chapter 4/5
	Oct. 17	Synchronous Sequential Logic	Chapter 5
	Fall Break (October 23-28)		
8	Oct. 29	Synchronous Sequential Logic	Chapter 5
	Oct. 31	Synchronous Sequential Logic + HDL	Chapter 5
9	Nov. 5	Synchronous Sequential Logic + HDL	Chapter 5
	Nov. 7	Registers and Counters	Chapter 6
10	Nov. 12	Registers and Counters + HDL	Chapter 6
	Nov. 14	Registers and Counters + HDL	Chapter 6
11	Nov. 19	Memory and Programmable Logic	Chapter 7
	Nov. 21	Memory and Programmable Logic	Chapter 7
12	Nov. 26	Asynchronous Sequential Circuits	Lecture notes
	Nov. 28	Asynchronous Sequential Circuits	Lecture notes
13	Dec. 3	Design and Test at the Register Transfer Level	Chapter 8
	Dec. 5	Design and Test at the Register Transfer Level	Lecture notes
		Fall Term Ends.	

Midterm

Topics (detailed)

1. Digital Systems and Binary Numbers:

Digital Systems, Binary Numbers, Number-Base Conversions, Octal and Hexadecimal Numbers, Complements of Numbers, Signed Binary Numbers, Binary Codes, Binary Logic.

2. Boolean Algebra and Logic Gates:

Basic Definitions, Axiomatic Definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms, Other Logic Operations, Digital Logic Gates, Integrated Circuits.

3. Gate-Level Minimization:

The Map Method, Product-of-Sums Simplification, Don't-Care Conditions, NAND and NOR Implementation, Other Two-Level Implementations, Hardware Description Languages (HDL).

4. Combinational Logic:

Combinational Circuits, Analysis of Combinational Circuits, Binary Adder-Subtractor, Decimal Adder, Binary Multiplier, Comparator, Decoder, Encoder, Multiplexer, HDL Models of Combinational Circuits, Behavioral Modeling and Simulation.

5. Synchronous Sequential Logic:

Sequential Circuits, Latches, Flip-Flops, Analysis of Clocked Sequential Circuits, Design Procedure State Reduction and Assignment, Synthesizable HDL Models of Sequential Circuits.

6. Registers and Counters:

Registers, Shift Registers, Ripple Counters, Synchronous Counters, Other Counters, HDL Models of Registers and Counters.

7. Memory and Programmable Logic:

Random-Access Memory, Read-Only Memory, Memory Decoding, Programmable Logic Devices.

8. Asynchronous Sequential Circuits:

Flow Table Analysis, Flow-Table Synthesis: The Toggle Circuit, Races and State Assignment.

9. Design at the Register Transfer Level:

Register Transfer Level (RTL) Descriptions, Algorithmic State Machines (ASMs), Race-Free Design Latch-Free Design.

General Regulations

- *Online Requirements*: Due to content currently being provided in an online capacity, students are required to have access to an internet connection.

- *Copyright on Course Materials*: The materials created for this course (including the course outline and any slides, online recorded classes, notes, program source code, labs, projects, assignments, quizzes, exams and solutions) are intended for personal use and may not be reproduced or redistributed or posted on any website without prior written permission from the author(s).

- *Attendance*: Students are expected to attend all lectures and lab periods. The University requires students to have a conflict-free timetable. For more information, see the current Undergraduate Calendar, Academic Regulations of the University, Section 1.2, Course Selection and Registration and Section 1.5, Deregistration.

- *Health and Safety*: Every student should have a copy of our Health and Safety Manual. A PDF copy of this manual is available online: http://sce.carleton.ca/courses/health-and-safety.pdf.

- *Deferred Term Work*: Students who claim illness, injury or other extraordinary circumstances beyond their control as a reason for missed term work are held responsible for immediately informing the instructor concerned and for making alternate arrangements with the instructor and in all cases, this must occur no later than three working days after the term work was due. The alternate arrangement must be made before the last day of classes in the term as published in the academic schedule. For more information, see the current Undergraduate Calendar, Academic Regulations of the University, Section 2.6, Deferred Term Work. Since students are required to have a stable and reliable internet connection, a poor internet connection will not be considered a sufficient reason to defer an online exam.

- *Appeal of Grades*: The processes for dealing with questions or concerns regarding grades assigned during the term and final grades is described in the Undergraduate Calendar, Academic Regulations of the University, Section 2.7, Informal Appeal of Grade and Section 2.8, Formal Appeal of Grade.

- *Academic Integrity*: Students should be aware of their obligations with regards to academic integrity. Please review the information about academic integrity at: https://carleton.ca/registrar/academic-integrity/. This site also contains a link to the complete Academic Integrity Policy that was approved by the University's Senate.

- *Plagiarism*: Plagiarism (copying and handing in for credit someone else's work) is a serious instructional offense that will not be tolerated.

- *Academic Accommodation*: You may need special arrangements to meet your academic obligations during the term. You can visit the Equity Services website to view the policies and to obtain more detailed information on academic accommodation at http://www.carleton.ca/equity/

Intellectual Property

Lectures and course materials prepared by the instructor are considered to be an instructor's intellectual property covered by the Copyright Act, RSC 1985, c C-42. These materials are made available to you for your own study purposes and cannot be shared outside of the class or "published" in any way. Lectures, whether in person or online, cannot be recorded without the instructor's permission. Posting course materials or any recordings you may make to other websites without the express permission of the instructor may constitute copyright infringement.

Classroom Conduct

- The classroom environment is premised on commitment to the following:
  - Professionalism
  - Respect
  - Honesty
  - Privacy

- In the context of in-person/online learning, students are expected to:
  - Represent themselves honestly in all communications, applications, assignments, tests, examinations, and other correspondence.
  - Respect the need of others to work in an environment that is conducive to learning in an online setting.
  - Be courteous and polite in all electronic exchanges with instructor and fellow classmates.
  - Be active and engaged participants in the learning process.
  - Respect the personal information and privacy of others.
  - Respect all copyright laws.

- While participating in this online/in-person course, students are encouraged to engage in appropriate behaviors. Inappropriate behaviors may include:
  - Using email or login account information that is not your own.
  - Engaging in any behavior that may be disruptive to other learners in the online learning environment.
  - Writing, using, sending, downloading, or displaying any information that is hostile, insulting to others, derogatory, obscene, harassing, threatening or otherwise offensive.
  - Reproducing course content or reposting course materials without explicit permission.