Instructor

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Office Hours : Tuesday/Thursday 10:30-11:30 ME5148

Academic Accommodations

Carleton guidelines processes for academic accommodation requests.

Special Information for Pandemic Measures

It is important to remember that COVID is still present in Ottawa. The situation can change at any time and the risks of new variants and outbreaks are very real. There are a number of actions you can take to lower your risk and the risk you pose to those around you including being vaccinated, wearing a mask, staying home when you're sick, washing your hands and maintaining proper respiratory and cough etiquette.

Feeling sick? Remaining vigilant and not attending work or school when sick or with symptoms is critically important. If you feel ill or exhibit COVID-19 symptoms do not come to class or campus. If you feel ill or exhibit symptoms while on campus or in class, please leave campus immediately. In all situations, you must follow Carleton's symptom reporting protocols.

Masks: Carleton has paused the COVID-19 Mask Policy, but continues to strongly recommend masking when indoors, particularly if physical distancing cannot be maintained. It may become necessary to quickly reinstate the mask requirement if pandemic circumstances were to change.

Vaccines: Further, while proof of vaccination is no longer required as of May 1 to attend campus or in-person activity, it may become necessary for the University to bring back proof of vaccination requirements on short notice if the situation and public health advice changes. Students are strongly encouraged to get a full course of vaccination, including booster doses as soon as they are eligible, and submit their booster dose information in cuScreen as soon as possible. Please note that Carleton cannot guarantee that it will be able to offer virtual or hybrid learning options for those who are unable to attend the campus.

All members of the Carleton community are required to follow requirements and guidelines regarding health and safety which may change from time to time. For the most recent information about Carleton's COVID-19 response and health and safety requirements please see the University's COVID-19 website and review the Frequently Asked Questions (FAQs). Should you have additional questions after reviewing, please contact covidinfo@carleton.ca.

Learning Objective

The objective of this course is to introduce the student to design of CMOS logic gates, digital circuit design using Verilog HDL and logic synthesis, asynchronous to synchronous interfacing, clock distribution and timing issues, digital circuit implementation and verification, digital memory and signaling technologies.

Learning Outcomes

A student who successfully fulfills the course requirements will have demonstrated an ability to:

1. define the three levels of abstraction used in digital design
2. design digital gates using NMOS, PMOS and CMOS logic families that implement boolean functions
3. define the voltage transfer characteristics of a digital inverter
4. design MUXes, latches and flip-flops using CMOS logic
5. design linear feedback shift registers (LFSRs) that produce pseudo-random bit patterns
6. design combinational and sequential logic circuits that can be synthesized using Verilog HDL
7. define setup time, hold time and propagation delay of a flip-flop
8. define synchronous and asynchronous signals
9. define metastability and its effects on the output of a flip-flop
10. design synchronization circuitry for interfacing asynchronous signals with synchronous circuits
11. define positive and negative skew
12. design circuits that perform effectively in the presence of clock skew
13. implement digital circuits using FPGAs
14. define digital verification and testing
15. define random access memory (RAM), read only memory (ROM) and electrically erasable programable read only memory (EEPROM)
16. use computer-aided tools in a lab environment with a lab partner to design, construct, simulate and test digital circuits
17. write lab reports, answer essay type questions using text, equations and numeric values for assignments and examinations

References

Jan Rabaey, *Digital Integrated Circuits*, Prentice Hall, 1996
S. Palnitkar, *Verilog HDL*, Prentice Hall, 1996
J. P. Hayes, *Introduction to Digital Logic Design*, Addison Wesley, 1993

Marking Scheme

Laboratory	30%	**Students must complete all labs**
Assignments	10%	
Midterm Exam	15%	Thursday Mar. 2nd, 2023 during class
Final Exam	40%	**Students have to pass the final exam to pass course**
Bonus Quizzes	10%	

TA name	TA email address	TA office location and

Week	Dates in 2023	Lectures	Labs	Assignments/Readings/Comments
0,1	Jan 9-20	Introduction & MOSFET		Labs start week of Jan 16-20
2	Jan 23-27	CMOS Logic Gates		Also some discussion on Asynchronous Circuits in preparation for labs
3	Jan 30-Feb 3	CMOS Logic Gates and Intro to Verilog HDL		Assignment 1, due Feb. 16 , 2023
4	Feb 6-10	Verilog HDL I		Introduction to Verilog Example verilog code
5	Feb 13-17	Verilog HDL II Sequential Circuits		Assignment 2, due March 2 , 2023
6	Feb 20-24			**Winter break no classes or labs**

7	Feb 27-Mar 3			**Review old midterm Feb 28 in class Midterm on Thur Mar 2 during class**
8	Mar 6-10	Digital Circuit Implementation		
9	Mar 13-17	Asynchronous		
10	Mar 20-24	System Clocking		Assignment 3, due April 6, 2023
11	Mar 27-31	Digital Design Verification		
12	April 3-7	Memory and Signal Technologies and Review		Friday April 7 holiday, no classes or labs, Friday's lab delayed until April 12
13	April 10-12	Review		April 12 follows Friday class schedule