



Carleton
UNIVERSITY

Department of Electronics
Faculty of Engineering, Carleton University,
Ottawa, Canada.

ELEC 4706 [0.5 credit]

High-Speed Electronics: Circuits and Systems

Course Description:

Challenges faced in designing high-speed electronic circuits and systems. Fundamentals of high-speed digital circuit design and data transfer architectures including timing, drivers, interface to high-speed components, channel modelling, power distribution, clock and data recovery. Hardware Description Language and CAD software laboratories.

Prerequisite: [ELEC 3500](#).

Lectures three hours a week, laboratory three hours alternate weeks.

Objective:

This course builds upon the digital and analog design knowledge acquired in preceding courses and addresses the major design challenges faced in high-speed digital system design. Operation at higher speed requires changes in design practices. Factors influencing new designs and architectures would be discussed. The design of digital integrated circuits has evolved into a fully automated process that starts with a behavioral or structural description of the circuit and uses synthesis as a link to a given implementation technology. The Hardware Description (HDL) simulation is a major part of the design process. This course will make use of HDL design and implement blocks of a Clock and Data Recovery (CDR) system and demonstrate hardware functionality using an FPGA. This approach is commonly used by engineers before subcomponents are integrated into an IC. Fundamentals of the HDL, event-driven simulator operation is discussed. High-speed data transfer properties, modeling, measurements, and techniques will be introduced to help understand the design specifications and implementation details of high-speed serial link circuits and systems.

The highest speed digital design uses transistor-levels models to implement transceiver blocks that process digital data transmitted over interconnect channels. The transmission is lastly performed by a serial interconnect where a single bit (or symbol) sends/received at a time. The concepts behind serial data transmission, SERDES, data rate, BER, eye-diagram, jitter, jitter tolerance, channel modeling, equalization, PLL, Clocking systems, CDR, etc. will be provided.



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Winter 2022, Arash Ahmadi

We will be covering the following topics, but not necessarily in this order:

❖ **High Speed System Design Fundamentals and VHDL**

1. Code Structure, Simulation, Synthesis
2. Concurrent Code, Combinational Circuits
3. Sequential Code, Sequential Circuits, State Machines
4. VHDL-AMS
5. High Speed System Design Fundamentals

❖ **High-Speed Design: Fundamentals**

1. Signal Quality
2. High-Speed Properties of Circuits and Components
3. Power: Distribution and Stability
4. Clock: Generation, Distribution, and Synchronization
5. High-Speed Memory and Memory Interface

❖ **Signal Integrity**

1. Electromagnetic Fundamentals for Signal Integrity
2. Transmission-Lines
3. Equalization
4. Crosstalk, Jitter and Noise
5. Network Analysis for High-Speed Digital Simulation and Design

Resources:

- *ELEC 4706 Course Notes and Lab Manual.*
- **Textbooks**
 1. Granberg, Tom. *Handbook of Digital Techniques for High-Speed Design: Design Examples, Signaling and Memory Technologies, Fiber Optics, Modeling, and Simulation to Ensure Signal Integrity.* Prentice Hall, 2004.
 2. Dally, William J., William J. Dally, and John W. Poulton. *Digital systems engineering.* Cambridge university press, 1998.
 3. Johnson, Howard W., and Martin Graham. *High-Speed Digital Design: A Handbook of Black Magic.* Vol. 155. Englewood Cliffs, NJ: Prentice Hall, 1993.
 4. Belous, Anatoly, and Vitali Saladukha. *High-Speed Digital System Design: Art, Science and Experience.* Springer Nature, 2019.
 5. Bogatin, Eric. *Signal and Power Integrity--Simplified.* Pearson Education, 2010.
 6. Huray, Paul G. *The Foundations of Signal Integrity.* John Wiley & Sons, 2009.
 7. Geoff Lawday et al. *A Signal Integrity Engineer's Companion.* Prentice Hall, 2008.
- **VHDL Resources:**
 1. Zwoliński, Mark. *Digital System Design with VHDL.* Pearson Education, 2004.
 2. LaMeres, Brock J. *Quick start guide to VHDL.* Springer, 2019.
 3. Bezerra, Eduardo Augusto, and Djones Vinicius Lettnin. *Synthesizable VHDL Design for FPGAs.* Switzerland: Springer International Publishing, 2014.



Instructor information

- Dr. Arash Ahmadi
- Office: Mackenzie Building 5146,
- Office Hours: by email appointment,
- Office Phone Number: 613-520-2600 ext. 4451
- Email: aahmadi@doe.carleton.ca

Graduate Assistant (GA) information:

	Name	Email	Office Hours
1	Yiteng Wang	yitengwang@cmail.carleton.ca	by appointment
2	Konrad Socha	konradsocha@cmail.carleton.ca	by appointment

Class and lab information

- Class Location: Southam Hall 316,
- Class Time: 10:00 AM - 11:30 AM Tuesday and Thursday
- Lab Time: refer to your schedule
- Pre-requisites, from the current Carleton University Undergraduate Calendars (<https://calendar.carleton.ca/undergrad/courses/ELEC/>).

Grading:

Method of Evaluation	% of Final Grade	Due Dates*
Lab Assignments (Individual)	30	Lab Days
Assignments (Individual)	10	During the Semester
Midterm Exam (Individual)	25	After Week 6 (TBA)
Final Exam (Individual)	35	TBA

Notes:

- The exams are for evaluation purposes only and will not be returned to the student.
- Health and Safety: See <https://carleton.ca/ehs/programs/working-lab/laboratory-health-and-safety/> for general guidelines.

Satisfactory term work

- In order to pass the course students must achieve *satisfactory performance* during the term.
- Satisfactory performance during the term requires:
 - Completion of all lab experiments,
 - A combined average grade more than 50% on lab reports,
 - A combined average grade more than 50% on assignments,
 - Midterms must be completed with a grade more than 30%,
 - The final exam must be completed with a minimum grade of 40% to pass the course.



Course Schedule

Please note the following course schedule is approximate.

Week	Date	Subject, activity, assignment, etc.	Textbook Chapter or Readings
1	Jan. 10	Introduction	Chapter
	Jan. 12	High Speed System Design Fundamentals and VHDL	
2	Jan. 17	High Speed System Design Fundamentals and VHDL	
	Jan. 19	High Speed System Design Fundamentals and VHDL	
3	Jan. 24	High Speed System Design Fundamentals and VHDL	
	Jan. 26	Electrical mode of wires in high-speed digital systems	
4	Jan. 31	LC Transmission Line Model	
	Feb. 2	Understanding the lossy line models	
5	Feb. 7	RLC Transmission Line Model	
	Feb. 9	Noise Sources in a Digital System	
6	Feb. 14	Crosstalk and Intersymbol Interference	
	Feb. 16	Managing Noise	
7	Feb. 21	Winter Break	
	Feb. 23	Winter Break	
8	Feb. 28	Circuit Design Techniques	
	Mar. 2	Circuit Design Techniques	
9	Mar. 7	Circuit Design Techniques	
	Mar. 9	Signaling in High-Speed Digital Circuits	
10	Mar. 14	Signaling in High-Speed Digital Circuits	
	Mar. 16	Timing in High-Speed Digital Circuits	
11	Mar. 21	Timing in High-Speed Digital Circuits: Synchronization	
	Mar. 23	Timing in High-Speed Digital Circuits: Timing circuits	
12	Mar. 28	Clock Distribution	
	Mar. 30	Power Distribution	
13	Apr. 4	Equalization	
	Apr. 6	Link Circuits and Architectures	
14	Apr. 11	Link Circuits and Architectures	
			Winter term ends.

Midterm
→

General Regulations

- *Online Requirements:* Due to content currently being provided in an online capacity, students are required to have a stable and reliable internet connection. It will not be possible to accommodate missed labs, or other deliverables due to a dropped internet connection. To reduce the chances of this impacting you it is recommended students use a wired internet connection where possible. Additionally, it is highly recommended students download the simulation software on their local computer so that should their internet connection drop they can complete a large amount of the work without it.
- *Copyright on Course Materials:* The materials created for this course (including the course outline and any slides, notes, program source code, labs, projects, assignments, quizzes, exams and solutions) are intended for personal use and may not be reproduced or redistributed or posted on any website without prior written permission from the author(s).
- *Attendance:* Students are expected to attend all lectures and lab periods virtually. The University requires students to have a conflict-free timetable. For more information, see the current Undergraduate Calendar, Academic Regulations of the University, Section 1.2, Course Selection and Registration and Section 1.5, Deregistration.
- *Health and Safety:* Every student should have a copy of our Health and Safety Manual. A PDF copy of this manual is available online: <http://sce.carleton.ca/courses/health-and-safety.pdf>.
- *Deferred Term Work:* Students who claim illness, injury or other extraordinary circumstances beyond their control as a reason for missed term work are held responsible for immediately informing the instructor concerned and for making alternate arrangements with the instructor and in all cases, this must occur no later than three (3.0) working days after the term work was due. The alternate arrangement must be made before the last day of classes in the term as published in the academic schedule. For more information, see the current Undergraduate Calendar, Academic Regulations of the University, Section 2.6, Deferred Term Work. Since students are required to have a stable and reliable internet connection, a poor internet connection will not be considered a sufficient reason to defer an online exam.
- *Appeal of Grades:* The processes for dealing with questions or concerns regarding grades assigned during the term and final grades is described in the Undergraduate Calendar, Academic Regulations of the University, Section 2.7, Informal Appeal of Grade and Section 2.8, Formal Appeal of Grade.
- *Academic Integrity:* Students should be aware of their obligations with regards to academic integrity. Please review the information about academic integrity at: <https://carleton.ca/registrar/academic-integrity/>. This site also contains a link to the complete Academic Integrity Policy that was approved by the University's Senate.
- *Plagiarism:* Plagiarism (copying and handing in for credit someone else's work) is a serious instructional offense that will not be tolerated.
- *Academic Accommodation:* You may need special arrangements to meet your academic obligations during the term. You can visit the Equity Services website to view the policies and to obtain more detailed information on academic accommodation at <http://www.carleton.ca/equity/>



Instructor's Policy on Recording Lectures

- Lectures in the virtual classroom will be recorded. The recordings will be posted in the course site, after the lecture. Students are not permitted to record the lectures.
- Any recording of lectures or guest lecturer/classmate presentations by students can be used only for the purposes of private study by the individual student. The recording (including any transcriptions or any translation to any other form) cannot be shared, distributed, emailed, posted online or otherwise disseminated or communicated in any form or to any other person (including fellow classmates) unless written consent has first been obtained from the instructor or presenter.
- Students who record a lecture after the instructor has prohibited such recordings, or who record a guest lecturer or classmate presentation or performance without the written consent of the presenter, or who disseminate a recording without the explicit written permission from the instructor or presenter will be subject to the University's misconduct policies, at minimum.
- Where the recording captures the image of classroom activities (e.g., video-recording, or other image-capture technology), such recording must only capture the instructor or the presenter within the classroom setting.

Intellectual Property

Lectures and course materials prepared by the instructor are considered to be an instructor's intellectual property covered by the Copyright Act, RSC 1985, c C-42. These materials are made available to you for your own study purposes and cannot be shared outside of the class or "published" in any way. Lectures, whether in person or online, cannot be recorded without the instructor's permission. Posting course materials or any recordings you may make to other websites without the express permission of the instructor may constitute copyright infringement.

Virtual Classroom Conduct

- The virtual classroom environment is premised on commitment to the following:
 - Professionalism
 - Respect
 - Honesty
 - Privacy
- In the context of online learning, students are expected to:
 - Represent themselves honestly in all communications, applications, assignments, tests, examinations, and other correspondence.
 - Respect the need of others to work in an environment that is conducive to learning in an online setting.
 - Be courteous and polite in all electronic exchanges with instructor and fellow classmates.
 - Be active and engaged participants in the learning process.
 - Respect the personal information and privacy of others.
 - Respect all copyright laws.
- While participating in this online course, students are encouraged to engage in appropriate behaviors. Inappropriate behaviors may include:
 - Using email or login account information that is not your own.



- Engaging in any behavior that may be disruptive to other learners in the online learning environment.
- Writing, using, sending, downloading, or displaying any information that is hostile, insulting to others, derogatory, obscene, harassing, threatening or otherwise offensive.
- Reproducing course content or reposting course materials without explicit permission.