ELEC 4708: Advanced Digital Integrated Circuits

Objectives

Lectures

Analysis, Design and Implementation of Modern VLSI Circuits and Systems

Labs

Use of a Modern IC Technology and Professional Cadence Tool for Designing a Circuit from a Functional Description to Final Chip Layout

Expected Learning Outcome

- VLSI Functionality, Speed, Energy and Reliability
- Device, Circuit, Logic and System Level Design
- Circuit Simulation, Layout Editor, HDL Design (RTL) and Chip Tape-out

Marking Scheme

Laboratory	**25%**	Attendance and performing all labs is mandatory. Not doing a single lab equals failure in course. No lab exemptions are given. Lab reports should be submitted online.
Quizzes	**7%**	Pop-up at the start of lectures
Assignments	**5%**	Expect 3 to 5
Midterm Exam	**18%**	Thu Oct 28, 2024
Final Exam	**45%**	Final Exam paper is for evaluation only, and will not be returned to students. Students have to pass the final exam to pass the course.

Topics

1. Review CMOS Logic
2. Review CMOS Latches and Flip-Flops
3. CMOS Layout
4. Review Hardware Description Language
5. MOSFET Current and Capacitances
6. Non-Ideal MOSFET Effects
7. CMOS Delay Estimation
8. Introduction to Logical Effort
9. Delay Optimization with Logical Effort
10. Power Estimation: Static and Dynamic
11. Low-Power Design
12. Static Combinational CMOS Logic Styles
13. Dynamic Combinational CMOS Logic Styles
14. Static and Dynamic Sequential Circuit Design
15. Testing and Design for Testability
16. Technology Scaling
17. VLSI Design Methodologies
18. VLSI Design Flow

Textbook

N. Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective," 4th Edition, Addison Wesley, 2011.

Reference

J. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits," 2nd Edition, Pearson Education, 2003.