Carleton University - Fall Term 2022-2023 - ELEC-5401

Signal Integrity in High-Speed Designs

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Course Objectives and Overview

1) To understand signal integrity issues in high-speed designs
2) To become knowledgeable of signal integrity and interconnect design/modeling/simulation methodologies

The rapid growth in VLSI circuit technology coupled with the trend towards complex/miniature devices is placing enormous demands on computer-aided design (CAD) tools focused on microelectronics. The design requirements are becoming very stringent, demanding higher operating speeds, sharper excitations, denser layouts and low power consumption. Consequently, signal integrity issues such as delay, attenuation, crosstalk, ground bounce etc. are becoming major bottlenecks in design and validation of high-speed circuits and systems.

High-speed effects, if not addressed properly during the design stage, can cause logic glitches which render a fabricated digital circuit inoperable, or they can distort an analog signal such that it fails to meet specifications. Since extra iterations in the VLSI design cycle are extremely costly, accurate prediction of these effects is a necessity in high-speed designs. A paradigm shift is currently taking place in both the design and CAD community to adapt to the new requirements of high-speed design issues. However, currently available CAD tools and design strategies do not handle the complex scenario of high-speed circuit design/analysis encompassing diverse domains, adequately.

This course would focus on understanding signal integrity issues, developing new generation CAD tools to model and simulate these effects, and also on developing design strategies to handle them. Following is a broad outline of the materials proposed to be covered in this course:

- Brief Review of Computer-aided Design for Circuit Analysis, Modified Nodal Analysis, Frequency Domain Analysis, Transient Analysis
- High-Speed Design and Signal Integrity Issues, Industry need/directions, signalling in design hierarchy: Chip, Package, PCB; Signal Integrity Practitioner’s View.
- Interconnect Parameters: Resistance, Capacitance, Inductance and Conductance. Related Concepts and parameter extraction.
- Distributed Interconnects: Telegraphers Equations, SPICE compatible frequency-domain stamps, mixed frequency/time analysis issues.
• Current Distribution Related Effects: Skin, Proximity and Edge Effects, Frequency-Dependent RLG parameters, Non-uniform Transmission lines, Full-wave models.
• Measurements: TDRs and VNAs, Multiport parameters, Concept and Underlying Theory of Scattering Parameters, Errors in the Data, Rational Function Based Macromodels, Vector-fit, SPICE compatible Realizations.
• System Architecture improvements for High-speed Channel Design, Serdes, Differential Signaling.

Books (recommended reading)

Also, additional hand-outs will be recommended in the class.

Prerequisites
Familiarity with the basic concepts in circuit theory/design, linear algebra and calculus.

Lecture Delivery: In person mode.

Grading
Assignments (2) 40%
In class Quizzes 10%
Final Exam 50%

Office Hours (3036 MC): Thu 4:30pm – 5:30pm.
Course Web-site: Elec5401 link in Carleton Brightspace