Carleton University

Department of Electronics

Winter 2025

ELEC 3500: Digital Electronics

Introduction

The objective of this course is to introduce the student to design of CMOS logic gates, digital circuit design using Verilog HDL and logic synthesis, asynchronous to synchronous interfacing, clock distribution and timing issues, digital circuit implementation and verification, digital memory and signaling technologies.

Course Description and Requirements

Course Description: Digital circuit design using verilog and logic synthesis, the electronic properties of logic gates, electrical interfacing between logic families, asynchronous to synchronous interfacing, clock distribution and timing, VLSI design options. Students implement substantial circuits with field-programmable gate arrays.
Includes: Experiential learning activity
Prerequisite(s): ELEC 2507 and ELEC 2607
Lectures: three hours a week
Laboratory and problem analysis: three hours a week

Instructor

Professor: Ralph Mason, Room ME5148
Email: ralphmason@cunet.carleton.ca
Course Webpage: on Brightspace

Textbook: Please include price of required books

1) Lecture notes are provided on Brightspace

2) Reference Textbook (not required): “Logic and Computer Design Fundamentals”, M. Mano, 5th ed.
Paperback $44.39 on thriftbooks, etextbook $64.99 at Pearson

Lecture Outline

In person, Wednesday & Friday. 14:35-15:55, ME3380
Office Hours: Wednesday & Friday 16:00-17:00, ME5148

The following topics will be covered during the course lectures with an approximate schedule:

Week	*Dates in 2025*	*Lectures*	*Labs*	*Assignments/Readings/Comments*
0,1	Jan 6-17	Introduction & MOSFET		Labs start week of Jan 13
2	Jan 20-24	CMOS Logic Gates		Also some discussion on Asynchronous Circuits in preparation for labs
3	Jan 27-31	CMOS Logic Gates and Intro to Verilog HDL		Assignment 1, due Feb. 14, 2025
4	Feb 3-7	Verilog HDL I		Introduction to Verilog Example verilog code
5	Feb 10-14	Verilog HDL II Sequential Circuits		Assignment 2, due Feb. 28, 2025
6	Feb 17-21			**Fall break no classes or labs**
7	Feb 24-28			**Review old midterm Feb. 26 in class** **Midterm on Friday Feb. 28 during class**
8	Mar 3-7	Digital Circuit Implementation		
9	Mar 10-14	Asynchronous		
10	Mar 17-21	System Clocking		Assignment 3, due April 4, 2025

11	Mar 24-28	Digital Design Verification and Memory and Signal Technologies		
12	Mar 31-Apr 4	Review		

Laboratory and Problem Analysis Sessions

3 hours (each week) as per schedule and location posted on Brightspace.

Notes for Labs

- There are 10 labs as follows:
  - Lab 0: Introduction (lab procedures and lab partner selection)
  - Lab 1: MOS Devices
  - Lab 2: Combination CMOS Logic
  - Lab 3: CMOS Sequential Logic Gates
  - Lab 4: Vivado Intro Tutorial and Verilog lab 1 – modelling concepts
  - Lab 5: Verilog lab 2 and 3 – Numbering systems, encoders, decoders and memories
  - Lab 6: Verilog lab 6 and 8 – registers, counters, architectural wizard and Intellectual Property (IP) catalog
  - Lab 7: Verilog lab 9 – Counters, timers and real-time clock
  - Lab 8: Verilog lab 10 – Finite State Machines (FSMs)
  - Lab 9: Egg Timer lab (note: this is a 2 week lab 1st week basic design, 2nd week add your innovations)

- Labs are 3 hours in duration and will be held in Room ME4275. Labs and PA sessions are most weeks and will be held according to the schedule shown on the course module in Brightspace. You must attend your lab in the session you are registered. Changing sessions is not allowed without the instructor's permission. A TA will take attendance at each lab session.
- If for some reason a Lab needs to be rescheduled OR a Lab falls on one of the University holidays, students in those sections must try to rearrange their schedule to make up the lab in another of the regularly scheduled lab sessions, as arranged by the instructor.
- Attend each lab punctually. Be prepared for the lab experiment by reading the lab instruction sheets before entering the lab. Some labs have a pre-lab exercise that must be completed before the start of your lab period. You are not permitted to do the lab unless the prelab is completed. The TA will check that the the pre-lab has been completed.
- A lab report will be submitted online for each lab group for labs 1, 2 and 3 and by each student for lab 9. A template for each lab report will be provided. Lab reports are due within 24 hours of the end of your lab session. Late lab reports must still be submitted. You must complete all labs (i.e. do not have a mark of 0 for any labs) to pass the course. Lab reports will be assessed a -25% penalty per week late.

Self-Declaration form and Deferred Term work

Students who claim illness, injury or other extraordinary circumstances beyond their control as a reason for missed term work are held responsible for immediately informing the instructor concerned and for submitting a self-declaration form no later than three (3) days after the date/deadline of term work including test/midterm, labs, assignments. Any alternate arrangements made with the instructor for submission of term work should be made as soon as possible but within 3 days of the missed due date. If this is not possible after discussion with the instructor, alternate arrangements must be made before the last day of classes in the term as published in the academic schedule.

Instructors can require (or not) the student to submit the self-declaration form. Include the following statement if you require the student to submit a completed self-declaration form:

> **Consult with the instructor no later then 3 days after any missed course work or midterm examination.**
>
> or
>
> **Contact the instructor with the completed self-declaration form no later than 3 days after the date/deadline of term work including test/midterm, labs, assignments.**

Evaluation and Grading Scheme

The cumulative course grade will be determined as follows:

- Laboratory 35% **Students must complete all labs**
- Assignments 10%
- Midterm Exam 15% Friday Feb. 28th 2025 during class
- Final Exam 40% **A minimum of 50% on the final exam is required to pass the course**
- Bonus Quizzes 10%

Final Exam -

- Final exam is for evaluation purpose and will not be returned to students.
- Final exam with be on campus and proctored using paper format
- Closed Book with a double sided 8”x11.5” crib sheet with scientific calculator
- Minimum grade on final exam to pass the course is 50%
- Final exam Weight is 40%
- Students who are unable to write the final examination because of a serious illness/emergency or other circumstances beyond their control may apply for accommodation by contact the Registrar’s office. Consult the Section 4.3 of the University Calendar (https://calendar.carleton.ca/undergrad/regulations/academicregulationsoftheuniversity/examinations/)

Midterm Exam –

- Closed Book with a double sided 8”x11.5” crib sheet with scientific calculator
- Midterm exam Weight is 15%

Additional Requirements -

- Students are required to complete all labs (i.e. must achieve at least part marks for all labs)

Learning Outcomes

The objective of this course is to introduce the student to design of CMOS logic gates, digital circuit design using Verilog HDL and logic synthesis, asynchronous to synchronous interfacing, clock distribution and timing issues, digital circuit implementation and verification, digital memory and signaling technologies.

Upon successful completion of this course, students will be able to:

1) define the three levels of abstraction used in digital design
2) design digital gates using NMOS, PMOS and CMOS logic families that implement boolean functions
3) define the voltage transfer characteristics of a digital inverter
4) design MUXes, latches and flip-flops using CMOS logic
5) design linear feedback shift registers (LFSRs) that produce pseudo-random bit patterns
6) design combinational and sequential logic circuits that can be synthesized using Verilog HDL
7) define setup time, hold time and propagation delay of a flip-flop
8) define synchronous and asynchronous signals
9) define metastability and its effects on the output of a flip-flop
10) design synchronization circuitry for interfacing asynchronous signals with synchronous circuits
11) define positive and negative skew
12) design circuits that perform effectively in the presence of clock skew
13) implement digital circuits using FPGAs
14) define digital verification and testing
15) define random access memory (RAM), read only memory (ROM) and electrically erasable programable read only memory (EEPROM)
16) use computer-aided tools in a lab environment with a lab partner to design, construct, simulate and test digital circuits
17) write lab reports, answer essay type questions using text, equations and numeric values for assignments and examinations

Graduate Attributes

The Canadian Engineering Accreditation Board requires graduates of undergraduate engineering programs to possess 12 attributes: Graduate-Attributes.pdf (engineerscanada.ca) or GA's. Courses in all four years of our programs evaluate students' progress towards acquiring these attributes. Aggregate data (typically, the data collected in all sections of a course during an academic year) is used for accreditation purposes and to guide improvements to programs. Some of the assessments used to measure GAs may also contribute to final grades; however, the GA measurements for individual students are not used to determine the student's year-to-year progression through the program or eligibility to graduate. Accreditation metrics are based on courses common to all students in a program.

This following list provides the GAs that will be measured in this course, along with the indicators that are intended to develop and assess these attributes.

Graduate Attribute and Level	**Indicators or Area for Specialization**	**Methods used for Evaluation**
GA-1 Knowledge base for Engineering Level 5	DOE- 5 Digital Circuits	Labs 2 & 3
GA-3 Investigation Level D	3.1 Complex problem assessment 3.2 Design of experiment 3.3 Experimental procedure 3.4 Data reduction methods and results 3.5 Interpretation of data (synthesis) and discussion	Labs 2 & 3
GA-4 Design Level D	4.1 Clear design goals	Lab 9

	4.2 Detailed design specifications and requirements 4.4 Design solution(s) 4.5 Design implementation/task(s) definition 4.6 Design: Alternate solution(s) definition and evaluation 4.7 Evaluation based on engineering principles	

Academic Integrity and Plagiarism

a) Please consult the Faculty of Engineering and Design information page about the Academic Integrity policy and our procedures: https://carleton.ca/engineering-design/current-students/fed-academic-integrity. Violations of the Academic Integrity Policy will result in the assignment of a penalty such as reduced grades, the assignment of an F in a course, a suspension or, expulsion.

b) One of the main objectives of the Academic Integrity Policy is to ensure that the work you submit is your own. As a result, it is important to write your own solutions when studying and preparing with other students and to avoid plagiarism in your submissions. The University Academic Integrity Policy defines plagiarism as "presenting, whether intentionally or not, the ideas, expression of ideas or work of others as one's own." This includes reproducing or paraphrasing portions of someone else's published or unpublished material, regardless of the source, and presenting these as one's own without proper citation or reference to the original source.

Examples of violations of the policy include, but are not limited to:

- Any submission prepared in whole or in part, by someone else;
- Using another's data or research findings without appropriate acknowledgment;
- Submitting a computer program developed in whole or in part by someone else, with or without modifications, as one's own;
- Failing to acknowledge sources of information through the use of proper citations when using another's work and/or failing to use quotations marks; and
- Unless explicitly permitted by the instructor in a specific course, the use of generative AI and similar tools to produce assessed content (such as text, code, equations, images, summaries, videos, etc.).

Academic Accommodations

You may need special arrangements to meet your academic obligations during the term. For an accommodation request the processes are as follows:

Pregnancy obligation: Contact us with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist. For accommodation regarding a formally-scheduled final exam, you must complete the Pregnancy Accommodation Form (click here).

Religious obligation: Contact us with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist. For more details click here.

Academic Accommodations for Students with Disabilities: The Paul Menton Centre for Students with Disabilities (PMC) provides services to students with Learning Disabilities (LD), psychiatric/mental health disabilities, Attention Deficit Hyperactivity Disorder (ADHD), Autism Spectrum Disorders (ASD), chronic medical conditions, and impairments in mobility, hearing, and vision. If you have a disability requiring academic accommodations in this course, please contact PMC at 613-520-6608 or pmc@carleton.ca for a formal evaluation. If you are already registered with the PMC, contact your PMC coordinator to send us your Letter of Accommodation at the beginning of the term, and no later than two weeks before the first in-class scheduled test or exam requiring accommodation (if applicable). After requesting accommodation from PMC, contact us, if needed, to ensure that accommodation arrangements are made.

You should request your academic accommodations in the Ventus Student Portal, for each course at the beginning of every term. For in-term tests or midterms, please request accommodations at least two (2) weeks before the first test or midterm.

Please consult the PMC website for the deadline to request accommodations for formally-scheduled exams (if applicable).

Survivors of Sexual Violence: As a community, Carleton University is committed to maintaining a positive learning, working and living environment where sexual violence will not be tolerated, and where survivors are supported through academic accommodations as per Carleton's Sexual Violence Policy. For more information about the services available at the university and to obtain information about sexual violence and/or support, visit: https://carleton.ca/equity/sexual-assault-support-services

Accommodation for Student Activities: Carleton University recognizes the substantial benefits, both to the individual student and for the university, that result from a student participating in activities beyond the classroom experience. Reasonable accommodation will be provided to students who compete or perform at the national or international level. Contact us with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist: https://carleton.ca/senate/wp-content/uploads/Accommodation-for-Student-Activities-1.pdf