Carleton University

Department of Electronics

Winter 2025

ELEC4706: High-Speed Electronics: Circuits and Systems

Introduction

This course builds upon the digital and analog design knowledge acquired in preceding courses.

The course addresses the significant design challenges faced by digital designers today. The HDL simulation is a major part of the design process. Fundamentals of the HDL and event-driven simulator operation are discussed. Operation at higher speed (digital chip up to 1GHz clock and mixed-signal digital chips up to 40GHz clock) changes design practices. Factors influencing these new designs will be discussed. The design of digital integrated circuits has evolved into a fully automated process that starts with a behavioural or structural description of the circuit and uses synthesis as a link to a given implementation technology.

High-speed electrical and optical channel properties, modelling, measurements, and communications techniques will be introduced to help understand the design specifications and implementation details of high-speed serial link circuits and systems such as drivers, receivers, equalizers, and synchronization systems. Link system design will be covered with an emphasis on understanding the challenges and some of the link architectures proposed to realize electrical and optical serial link standards.

The highest-speed digital design does not follow this route; it uses transistor-level design. It is called a “mixed-signal” design and includes transceiver blocks that process digital data transmitted over interconnect channels. The transmission is lately performed by a serial interconnect where a single bit (or symbol) is sent/received at a time. The concepts behind serial data transmission (data rate, BER, eye diagram, jitter, jitter tolerance, etc.) and examples of transmitter, channel and receiver devices will be provided.

Course Description and Requirements

Course Description: Challenges faced in designing high-speed electronic circuits and systems. Fundamentals of high-speed Tx/Rx architectures, including timing and HDL, PLL/DLL, Tx drivers, interface to photonic components, channel modelling, Rx channel, choice of modulation, equalization, clock and data recovery. VHDL hardware and CAD software laboratories
Prerequisite(s): ELEC 3500.
Lectures: 3 hours per week.
Laboratory and problem analysis: 3 hours per week

Instructor

Professor: Rony E. Amaya
Email: rony.amaya@carleton.ca
Course Webpage: on Brightspace

Textbook and References:

1) ELEC 4706 Course Notes and Lab Manual (Main source and available on bright space)
2) William Dally, Digital Systems Engineering; Cambridge Publishing ;ISBN-13:978-0521061759 -;ISBN-10:052106175X (Strong reference but not required)

Additional References (not required):

3) B. Razavi, Design of Integrated Circuits for Optical Communications , Wiley - ISBN-10:1118336941
4) Charles Roth, Digital Systems Design using VHDL , Thompson Engineering -ISBN-10: 0534384625 -ISBN-13: 978-0534384623
5) Michael D. Ciletti; Modelling and Synthesis and Rapid Prototyping with te Verilog HDL; Prentice Hall, 1999
6) Janick Bergeron; Writing Testbenches – Functional verification of HDL models; Springer 2003
7) Steven Brown, Zvonko Vrasenic; Digital Logic with VHDL Design; McGrawHill 2009
8) J. Bashker; A VHDL Primer; Prentice Hall; 1995
9) Geoff Lawday et al. A signal Integrity Engineer's Companion; Prentice Hall 2008
10) Eric Bogatin; Signal and Power Integrity; Prentice Hall 2010
11) Sudhar Yalamanchili; VHDL Starter's Guide; Prentice Hall 1998
12) Kenneth L. Short; VHDL for beginners; Prentice Hall 2009

Lecture Outline

In person, Tuesdays and Thursdays 11:35 to 12:55 in SA 517.
The following topics will be covered during the course lectures with an approximate schedule:

Week 1: Intro to High-Speed Electronics – Circuits and Systems.
Week 2: Intro to VHDL.
Week 3: Challenges in Optical Communications and Digital System Engineering.
Week 4: Channel modelling - lossy wires, buses, balanced lines, Noise, ISI.
Week 5: Signaling across the channel.
Week 6: Communication Techniques.
Week 7: Equalizers.
Week 8: Tx/Rx Circuits.
Week 9: Clocking Systems.
Week 10: Link Modeling.
Week 11: Link Examples.
Week 12: Final Review.

Laboratory and Problem Analysis Sessions

3 hours (every week) as per schedule and location posted on Brightspace.

Lab schedule:

Group A2: Tuesdays, 08:35 - 11:25 in ME4135.

Group A1: Fridays, 11:35 - 14:25 in ME4135.

Notes for Labs

- There are EIGHT labs as follows:
  - Lab 1: Introduction to FPGA Design Flow.
  - Lab 2: Timing Analysis and Library Modules.
  - Lab 3: Array Multiplier.
  - Lab 4: On-Chip Memory.
  - Lab 5: PRBS Generator.
  - Lab 6: SERDES (Part 1): Oversampling CDR.
  - Lab 7: SERDES (Part 2): System Integration and Verification.
  - Lab 8: SERDES (Part 3): Hardware Implementation.

- Labs are 3 hours long and will be held in Room ME4135 according to the schedule shown on the course module in Brightspace. You must attend your lab in the session you are registered. Changing sessions is not allowed without the instructor's permission. A TA will take attendance at each lab session.
- If for some reason a Lab needs to be rescheduled OR a Lab falls on one of the University holidays, students in those sections must try to rearrange their schedule to make up the lab in another of the regularly scheduled lab sessions, as arranged by the instructor.
- Attend each lab punctually. Be prepared for the lab experiment by reading the lab instruction sheets before entering the lab. Some labs have a pre-lab exercise that must be completed before the start of your lab period. You are not permitted to do the lab unless the prelab is completed. The TA will check that the the pre-lab has been completed.
- A lab report will be submitted online for each lab and by each student. A template for each lab report will be provided. Lab reports are due by 11:30 pm on the day of the lab. Late lab reports must still be submitted. One day late it will only be worth 50%. Two days late, it is worth 0. **YOU MUST SUBMIT ALL LABS WITH A GRADE OF AT LEAST 50% TO PASS THE COURSE**.

Notes for Assignments

- Several assignments will be provided to help understand the lecture material and prepare for the final exam. To learn the course material. **YOU MUST SUBMIT ALL ASSIGNMENTS WITH A GRADE OF AT LEAST 50% TO PASS THE COURSE**.

Self-Declaration form and Deferred Term work

Students who claim illness, injury or other extraordinary circumstances beyond their control as a reason for missed term work are held responsible for immediately informing the instructor concerned and for submitting a self-declaration form no later than three (3) days after the date/deadline of term work including test/midterm, labs, assignments. Any alternate arrangements made with the instructor for submission of term work should be made as soon as possible but within 3 days of the missed due date. If this is not possible after discussion with the instructor, alternate arrangements must be made before the last day of classes in the term as published in the academic schedule.

Consult with the instructor no later then 3 days after any missed course work or midterm examination.

or

Contact the instructor with the completed self-declaration form no later than 3 days after the date/deadline of term work including test/midterm, labs, assignments.

Evaluation and Grading Scheme

The cumulative course grade will be determined as follows:

- Laboratory: 40%
- Assignments: 10%
- Final Exam: 50%

- All labs and assignments must be completed with a 50% or better grade to pass the course.
- At least 50% on the final exam is required to pass the course.
- As per standard practice in the Faculty of Engineering, students cannot see their final exams.
- Academic accommodation must be sought as soon as possible, preferably early in the term. Verification will be required.

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a) Final Exam: **Final exams are for evaluation purpose and will not be returned to students.**

ii) Closed-book exam. Calculators, self-contained, non-graphing, memory cleared. Double-sided 8.5" x 11" crib sheet with equations ONLY.

iii) Final exam weight: 50%. You MUST score at least 50% in the Final Exam to pass the course.

iv) Deferred Final Examinations

Students who are unable to write the final examination because of a serious illness/emergency or other circumstances beyond their control may apply for accommodation by contact the Registrar's office. Consult the Section 4.3 of the University Calendar (https://calendar.carleton.ca/undergrad/regulations/academicregulationsoftheuniversity/examinations/)

b) Additional requirement(s):

Please consult Section 5 of the undergraduate regulations (https://calendar.carleton.ca/undergrad/regulations/academicregulationsoftheuniversity/grading/)

If additional requirements beyond the cumulative grade earned in the course (for example, a requirement that students complete/pass certain assignments, examinations, lab, project components, or attend a minimal number of lab/PA sessions in order to pass the course), this should be clearly identified in the course outline.

c) Exam format and e-proctoring statement

Engineering Courses shall have on campus and proctored final examinations.

Learning Outcomes

Upon successful completion of this course, students will be able to:

1) Understand High-Speed Electronic systems.
2) Identify the challenges with High-Speed Electronic systems: noise, distortion, signalling, clock distribution, technologies, SERDES, CDR and Equalization.
3) Understand noise limitations in High-Speed Electronic systems.
4) Acquire a system-level understanding of PLL, DLL, and clock distribution in High-Speed Electronic systems.
5) Understand and calculate required Rx equalization in High-Speed Electronic systems.
6) Understand and calculate required Tx equalization in High-Speed Electronic systems.
7) Reinforce understanding of VHDL and use in programming FPGAs.
8) Complete the design, implementation and experimental testing of a SERDES link using an FPGA.

Academic Integrity and Plagiarism

a) Please consult the Faculty of Engineering and Design information page about the Academic Integrity policy and our procedures: https://carleton.ca/engineering-design/current-students/fed-academic-integrity. Violations of the Academic Integrity Policy will result in the assignment of a penalty such as reduced grades, the assignment of an F in a course, a suspension or, expulsion.

b) One of the main objectives of the Academic Integrity Policy is to ensure that the work you submit is your own. As a result, it is important to write your own solutions when studying and preparing with other students and to avoid plagiarism in your submissions. The University Academic Integrity Policy defines plagiarism as "presenting, whether intentionally or not, the ideas, expression of ideas or work of others as one's own." This includes reproducing or paraphrasing portions of someone else's published or unpublished material, regardless of the source, and presenting these as one's own without proper citation or reference to the original source.

Examples of violations of the policy include, but are not limited to:

- Any submission prepared in whole or in part, by someone else;
- Using another's data or research findings without appropriate acknowledgment;
- Submitting a computer program developed in whole or in part by someone else, with or without modifications, as one's own;
- Failing to acknowledge sources of information through the use of proper citations when using another's work and/or failing to use quotations marks; and
- Unless explicitly permitted by the instructor in a specific course, the use of generative AI and similar tools to produce assessed content (such as text, code, equations, images, summaries, videos, etc.).

Academic Accommodations

You may need special arrangements to meet your academic obligations during the term. For an accommodation request the processes are as follows:

Pregnancy obligation: Contact us with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist. For accommodation regarding a formally-scheduled final exam, you must complete the Pregnancy Accommodation Form (click here).

Religious obligation: Contact us with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist. For more details click here.

Academic Accommodations for Students with Disabilities: The Paul Menton Centre for Students with Disabilities (PMC) provides services to students with Learning Disabilities (LD), psychiatric/mental health disabilities, Attention Deficit Hyperactivity Disorder (ADHD), Autism Spectrum Disorders (ASD), chronic medical conditions, and impairments in mobility, hearing, and vision. If you have a disability requiring academic accommodations in this course, please contact PMC at 613-520-6608 or pmc@carleton.ca for a formal evaluation. If you are already registered with the PMC, contact your PMC coordinator to send us your Letter of Accommodation at the beginning of the term, and no later than two weeks before the first in-class scheduled test or exam requiring accommodation (if applicable). After requesting accommodation from PMC, contact us, if needed, to ensure that accommodation arrangements are made.

You should request your academic accommodations in the Ventus Student Portal, for each course at the beginning of every term. For in-term tests or midterms, please request accommodations at least two (2) weeks before the first test or midterm.

Please consult the PMC website for the deadline to request accommodations for formally-scheduled exams (if applicable).

Survivors of Sexual Violence: As a community, Carleton University is committed to maintaining a positive learning, working and living environment where sexual violence will not be tolerated, and where survivors are supported through academic accommodations as per Carleton's Sexual Violence Policy. For more information about the services available at the university and to obtain information about sexual violence and/or support, visit: https://carleton.ca/equity/sexual-assault-support-services

Accommodation for Student Activities: Carleton University recognizes the substantial benefits, both to the individual student and for the university, that result from a student participating in activities beyond the classroom experience. Reasonable accommodation will be provided to students who compete or perform at the national or international level. Contact us with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist: https://carleton.ca/senate/wp-content/uploads/Accommodation-for-Student-Activities-1.pdf