Carleton University Department of Electronics

Fall 2025

ELEC 2607: Switching Circuits

Introduction

This course covers the analysis, design and Implementation of modern VLSI Circuits and Systems. Labs use a modern IC technology kit and the professional Cadence tool for circuit simulations, layout editing, and synthesis and implementation of a circuit from a functional description to the final chip layout.

Course Description and Requirements

Advanced Verilog, test benches. VLSI design based on CMOS technology, characteristics of CMOS logic circuits, cell libraries, building blocks, structured design, testing, Computer-Aided Design tools. Laboratory emphasis on design synthesis from Verilog.

Prerequisite(s): fourth-year status in Engineering and ELEC 3500 or permission of the department
Lectures: three hours a week
Laboratory: laboratory and problem analysis three hours alternate weeks

Instructor

Professor Maitham Shams, Room ME4156
Email: MaithamShams@cunet.carleton.ca
Course Webpage: on Brightspace

Textbook

1) Lecture slides/notes are provided on Brightspace
2) Notes written on the board
3) Textbook: Neil Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Fourth Edition, Addison Wesley, 2011

Lecture Outline

In person, Tuesdays and Thursdays, 10:05-11:25, ME3356
The following topics will be covered during the course lectures with an approximate schedule.

Week 1: Introduction to digital ICs
Week 2: MOSFET basic structure, operation, and fabrication
Week 2: CMOS inverter and basic logic gates
Week 3: Compound CMOS logic gates and storage elements (latches and flip-flops)
Week 4: Brief history of ICs, CMOS layout rules, stick diagram, and layout-size estimation

Week 5: Long channel, ideal CMOS transistor theory, current and capacitances
Week 6: Short-channel non-ideal MOS behaviour, current, threshold voltage, leakage
Week 7: Process-Voltage-Temperature (PVT) variations, and simulation corners
Week 8: DC response of CMOS inverter, VTC, Noise margins (reliability)
Week 9: Transient response of CMOS inverter, RC delay model, Elmore's approximation
Week 10: Delay estimation and optimization with logical effort
Week 11: Dynamic and static power estimation and reduction
Week 12: CMOS static and dynamic circuit families

Laboratory and Problem Analysis Sessions

3 hours per week as per schedule and location posted on Brightspace.

- There are three labs as follows:
  - Lab 1: NAND gate layout extraction and simulation
  - Lab 2: Delay optimization using logical effort (decoder circuit)
  - Lab 3: Synthesis and chip design (signed multiplier)

- Labs are 3 hours in duration and will be held in MC6030. Labs and PA sessions usually "alternate" from week to week and will be held according to the schedule shown on the course module in Brightspace. You must attend your lab in the session you are registered. Changing sessions is not allowed without the head TA's permission.

- If for some reason a Lab needs to be rescheduled OR a Lab falls on one of the University holidays, students in those sections must try to rearrange their schedule to make up the lab in another of the regularly scheduled lab sessions, as arranged by the instructor.

- Attend each lab punctually. Be prepared for the lab experiment by reading the lab instruction sheets before entering the lab. Some labs have a pre-lab exercise that must be submitted by the due dates specified on Brightspace. You are not permitted to do the lab unless the prelab is completed. The TA will check that the the pre-lab has been completed.

Evaluation and Grading Scheme

The cumulative course grade will be determined as follows.

Laboratory	25%	Attendance and working on all labs are mandatory. Not doing a single lab equals failure in the course. No lab exemptions are given. Lab reports should be submitted online.
Quizzes	12%	Pop-up
Assignments	0%	Expect 3 to 5
Midterm Exam	18%	Tue Oct 28, 2025, class time
Final Exam	45%	Final Exam paper is for evaluation only and will not be returned to students. Students must pass the final exam to pass the course.

Important Notes:

- Lab exemptions cannot be granted due to accreditation requirements.

- Students are required to complete all lab sessions and must achieve a minimum of 50% in their overall lab marks to pass the course. Missing even one lab will fail the course.
- To pass the course, students must obtain at least 50% in their term mark (which includes labs, assignments, and the midterm) and a minimum of 50% on the final examination.
- Final exam papers will not be returned to students.

Learning Outcomes

A student who successfully fulfills the course requirements will have demonstrated the following knowledge and skills.

1. Understand CMOS digital circuits functionality, speed, energy consumption and reliability
2. Have very good knowledge of the structure and operation of MOSFETS
3. Design CMOS digital Circuit at different levels of abstraction from logic to system level
4. Perform circuit simulation, edit and extract layout, design modules and synthesis using HDL
5. Ready for job interviews in related fields

Graduate Attributes

None for this course.