ELEC 4609 Integrated Circuit Design and Fabrication

Instructor: Prof. Rony E. Amaya
email: rony.amaya@carleton.ca
Lectures: Tue, Thu 11:35 -12:55 SA 311 (IN-PERSON)
Office Hours: By Appointment - ONLINE or IN-PERSON
Team Channel: General | ELEC4609F2026
Discord Channel: https://discord.gg/CJXg2Y3TdD

TAs:
Patrick Ferenc
Lab: Every week- MC6030, Monday 11:35 - 14:25
TA Office Hours: **By Appointment - ONLINE on IN-PERSON**

Marking Scheme

Final exam 50% (The final exam is for evaluation only and will not be returned)

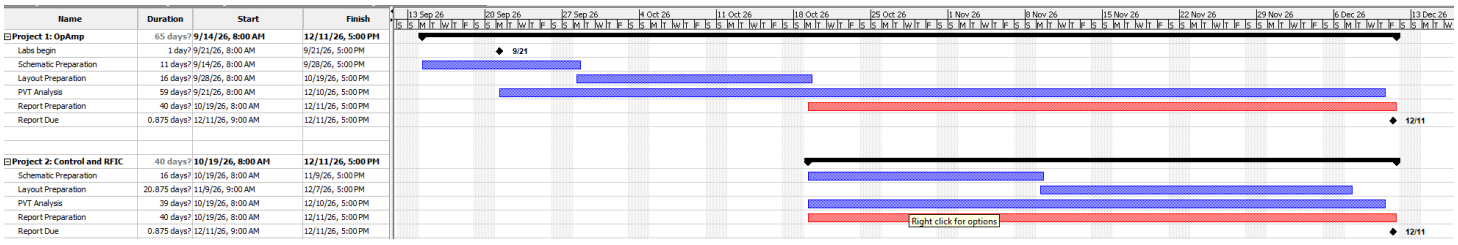
CMOS IC OpAmp project #1: 25% (MANDATORY TO PASS THIS COURSE)

CMOS IC Project #2: 25% (MANDATORY TO PASS THIS COURSE)

Assignments and Quizzes: 0% (MANDATORY TO PASS THIS COURSE - IT WILL NOT BE GRADED)

IC Design Projects

The TWO most important components of ELEC4609 are the IC design projects : Project #1) Layout and PVT verification of an Operational Amplifier based circuit and Project #2) Several follow up projects that makes use of the OpAmp in project #1 to build control circuits that would include a) A bandgap reference circuit, b) a voltage regulator (LDO) c) a Voltage Controlled Oscillator (VCO) with an integrated LDO (For those interested in RFIC and with relevance to FYP). For part 1), students will use a state-of-the-art CMOS process and design and verify an operational amplifier meeting required specifications. Students are encouraged to work in pairs on part 1) and submit a single report. Each member of the team must understand all aspects of the design and clearly identify his/her contributions to the report. To give students a glimpse into the life of an IC designer, there will be tight deadlines for the design submission. Project #2 sign-up should be completed by the end of the lab on October 5. Project #2 will follow a similar schedule and deliverables. A complete schedule for the two projects, is shown below. TWO reports are due on the last day of classes (TWO projects and ONE report for each group).



Assignments and Labs

The Two IC project sections require many hours of work with CAD tools, which will inevitably be done outside scheduled lab periods. All labs will be delivered in person. TAs and the course instructor will provide technical

assistance remotely as well as provide live demos. The formally scheduled lab periods allow a TA to review and comment on your work. Lab 1 will give a tutorial introduction to the CAD tools we will use. In addition to the term IC design project, there will be several assignments on the fundamentals of CMOS process design. Formal labs begin Sep. 21 and will run every week in MC6030. You are strongly encouraged to start working on Lab 1 before that date. For access to Cadence and/or technical tool issues, contact scott.bruce@carleton.ca.

Topics:

1. Circuits and Layout

Basic CMOS structure and process flow. The relationship between layout and cross-section. Design rules. Introduction to CAD tools for schematic capture, circuit simulation (SPICE) and layout. CMOS inverter: transfer characteristic, ratioing, noise margin, rise and fall times. Advantages of CMOS. NAND and NOR gates. Transmission gates. Dynamic logic. Input protection. Driving large capacitive loads with output buffers. Latch-up. Introduction to analog CMOS circuits: differential amplifiers, source follower buffers, current mirrors, device matching, temperature compensation.

2. Op-Amp circuit design, layout and verification

Fundamentals of Op-Amp design, current mirrors, input differential pair, output stages. Gain and stability including pole-splitting. Advance analysis including PSRR, phase margin and more. Analog Circuit Layout fundamentals including matching, symmetry, common-centroid, and others. Full Analog verification including post-layout extraction, Analysis under PVT variations. DRC. LVS verification using commercial software.

2. Op-Amp based circuit design, layout and verification

Op-Amp based circuits will include Bandgap references, LDO regulators, RFIC Voltage Controlled Oscillators (VCO). Circuit implementation of these blocks will also include exposure to temperature sensors, DACs, SPI interface and other required blocks in a commercial IC setting.

3. CMOS Process Technology (If time permits)

Overview of the processes required to fabricate a MOS IC: oxidation, ion implantation, diffusion, thin film deposition, photolithography, and etching. Integration of basic steps into a simple CMOS process flow. Short channel effects, hot carrier effects, and techniques for suppression. Evolution of CMOS technology: shallow trench isolation, high-k dielectrics, strained silicon... The future of microelectronics.

Recommended (but not compulsory) textbook:

R. Jacob Baker, Harry W. Li, and David E. Boyce, CMOS: Circuit Design, Layout, and Simulation, 3rd ed, 2010 IEEE Press, ISBN 0-7803-3416-7 (can be ordered online through IEEE or Chapters)

Alan Hastings: The Art of Analog Layout, 1st ed, 2000. ISBN-10:0130870617 (can be ordered online through IEEE or Chapters)

Calvin Plett, John W.M. Rogers: Radio Frequency Integrated Circuit Design, Second Edition, Copyright: 2010, ISBN: 9781607839804.

Health and Safety

See http://www.doe.carleton.ca/undergrads/health-and-safety.pdf for general Health and Safety: See http://www.doe.carleton.ca/undergrads/health-and-safety.pdf for general guidelines. Normal precautions in working with low-voltage electrical equipment must be taken when testing projects. Students volunteering to assist in multi-project chip fabrication in the Carleton Microfab must complete special training and must be WHMIS qualified.

Plagiarism

Plagiarism is a severe instructional offence that will not be tolerated. It involves passing off someone else's original work as your own. Most cases of plagiarism can be avoided by carefully citing sources for any ideas, statements, results etc. that are not your own. For additional information, please refer to the section on instructional offences in the Undergraduate Calendar.

The use of generative AI tools (such as ChatGPT) in coursework is prohibited unless explicitly authorized by the course instructor for specific course elements.

Academic Accommodation

You may need special arrangements to meet your academic obligations during the term. For an accommodation request the processes are as follows:

Pregnancy obligation**:** write to me with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist. For more details visit the Equity Services website: http://carleton.ca/equity/accommodation/student_guide.htm

Religious obligation**:** write to me with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist. For more details visit the Equity Services website: http://carleton.ca/equity/accommodation/student_guide.htm

Students with disabilities requiring academic accommodations**:** in this course must register with the Paul Menton Centre for Students with Disabilities (PMC) for a formal evaluation of disability-related needs. Documented disabilities could include but are not limited to mobility/physical impairments, specific Learning Disabilities (LD), psychiatric/psychological disabilities, sensory disabilities, Attention Deficit Hyperactivity Disorder (ADHD), and chronic medical conditions. Registered PMC students are required to contact the PMC, 613-520-6608, every term to ensure that I receive your *Letter of Accommodation*, no later than two weeks before the first assignment is due or the first-in-class test/midterm requiring accommodations. If you only require accommodations for your formally scheduled exam(s) in this course, please submit your request for accommodations to PMC by the last official day to withdraw from classes in each term. For more details visit the PMC website: http://www.carleton.ca/pmc/students/acad_accom.html