

MicroFabrication Facility

(CUMFF) Faculty of Engineering and Design, Department of Electronics



CUMFF Class 100 Cleanroom area

The Carleton University MicroFabrication Facility is a class 100 to 10,000 - 3200 square foot cleanroom facility used for manufacturing silicon integrated circuits and other device materials in support of research on: process technology, device physics/modeling, innovative circuit techniques, photonics, biomedical devices, renewable energy (solar cells) and micro-electromechanical systems (MEMS).

While the facility's primary objective is to support Carleton graduate student research and fabricate annual undergraduate projects, external academic and industrial users/partners are also welcome to access the lab and equipment for research work, small-volume production runs or start-up processing.

The CUMFF industry trained lab staff can assist in process development and project processing.

A notable strength of the CUMFF is in MOS processing; MOS gate dielectrics can be produced with contamination at industry acceptable levels. To illustrate this capability, every year the CUMFF lab is used in a quasi-production mode to fabricate student submitted designs on a multiproject chip from layout to completed chip. The project uses 5μ m LOCOS-isolated polysilicon gate nMOS technology, and more recently cMOS technology on SOI material.

These designs typically contain 50 to 100 transistors. Working chips are returned for testing within approximately three weeks of submission of CAD files, and wafer-level probing usually indicates yields of over 80% for the circuits.



Facility Layout

The Microfabrication Facility is located on the 4th floor of the Minto Center for Advanced Engineering building and has a total clean room floor area of approximately 3200 ft². The lab contains four distinct working areas for photolithography, photomask preparation, furnace operations, and high vacuum processes, each separated by a service bay. A separate air conditioning system maintains the facility temperature at 20°C with 40% relative humidity

throughout the year. Class 100 air quality is maintained in the photolithography and photomask production areas (approximately 80 m^2 total), Class 1,000 in the vacuum system area and class 10,000 in the oxidation/diffusion area.

Photomask Generation



Photomasks are generated in-house from CIF files using a David Mann 3000 pattern generator system, and a Jade step-and-repeat camera providing 10X reduction. Both the pattern generator and the step-and- repeat camera use high resolution silver halide emulsion photographic plates. The pattern generator can resolve 4 μ m features with 4 μ m spacing. The minimum feature size obtainable with the stepand-repeat camera is approximately 1.5 μ m, limited primarily by the grain size of the photographic plates. Chrome photomasks are available through external vendors.

Photolithography

Photolithography is carried out using a Karl-Suss MA6 UV mask aligner, which can accept substrates ranging from small fragments to 100 mm diameter wafers. Feature sizes down to 0.8 μ m have been printed using chrome masks. A HMDS vapor oven, photoresist spinners, bake ovens, hotplates and developing benches are used for the photoresist processing.

Oxidation/Diffusion



An eight-stack Bruce Model BDF-8 furnace bank is available for thermal processing up to 1200 C on wafers up to 100 mm in diameter. Tubes for oxidation, implant annealing and drive-in, phosphorus predeposition and hydrogen metal sinter are operational. Gettering with HCl gas is used before all oxidation cycles to control Na+ ionic contamination. With this precaution it is possible to produce gate oxides showing effectively no flatband shift in bias-temperature stress tests.

LPCVD/PECVD

A four-stack Bruce furnace bank is used for Low **P**ressure Chemical Vapor **D**eposition. Depositions include: LPCVD Oxides (doped and undoped), BPSG, Amorphous Silicon and PolySilicon, and Silicon Nitride. A Trion Orion III PECVD system used for PECVD Silicon Nitride, Silicon dioxide and hydrogenated silicon films on up to 8" wafers.

Cleaning and Wet Etching

Several wet benches with exhaust and cascade rinsers are available throughout the lab for wet chemical processing and cleaning.. Ultrapure18 Mega ohm DI (De-ionized) water is produced onsite, stored in a 200 gallon tank and continuously re-circulated throughout the lab to maintain purity. Clean DI water is essential for the production of semiconductor devices.

Plasma Etching



Several dry etch systems are available in the Microfabrication Lab. A MRC RIE 61 reactive ion etcher is used for oxide etching, including sidewall spacer formation. Vertical-walled optical waveguides 10 μ m high have been etched in deposited SiO₂ layers to form optical waveguides. Other plasma etch systems include a Technics Planar Etch II ,a March RIE etcher and 2 microwave plasma etchers for resist stripping.

Metallization and Thin Films



Several multi-purpose metal deposition systems are available: A loadlocked inline Semicore sputtering system with sputter etch capability, two ebeam/thermal evaporator systems, and a Varian M2000 single chamber RF/DC sputter system. A number of different materials can be deposited including Al, Ti, Au, Ag, SiO₂, Cr, Pt etc.

Access to Atomic Layer Deposition processing (ALD), is available through the newly opened Facility for Nanostructures, Surfaces, and Sensor Interfaces (FANSSI) facility on the 5th floor of the Minto Building. This new Chemistry/Electronics shared facility includes a wetlab and a class 10,000 cleanroom lab. The equipment set includes a Picosun Atomic Layer deposition system, a Angstrom Engineering Thermal Evaporation system housed inside a Mbraun high purity glovebox, and a Trion PECVD system.

Process Monitoring



Optical microscopes are available throughout the lab for optical inspections, taking photographs and making linewidths measurements if necessary. Ellipsometers,profilometers, and an AFM Atomic Force Microscope are available for film thickness and characterization. A Jeol Scanning electron microscope is available for SEM imaging. A CV test station consisting of a hot chuck with a CV meter is available to test gate dielectric quality.

Dicing/wirebonding/testing

Wafer dicing, wirebonding and testing equipment is also available for non-production type projects. <u>CUMFF Contacts:</u>

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