



Carleton
UNIVERSITY

Department of
**Systems and
Computer Engineering**

SYSC 4507

Computer Systems Architecture

Calendar description

Evolution of computer systems architecture, influences of changing technology, techniques to improve performance, memory hierarchy, hardware accelerators. Instruction level parallelism, pipelining, vector processing, superscalar, out of order execution, speculative execution. Thread level parallelism, multi-core, many-core, heterogeneous systems. Evolution of architectures for specific application domains.

Includes: Experiential Learning Activity.

Lectures three hours a week, laboratory/problem analysis one hour a week.

<http://calendar.carleton.ca/undergrad/courses/SYSC/>

Prerequisites

ELEC 2607 and (SYSC 2001 or SYSC 3006).

Precludes additional credit for SYSC 4310.

Prior knowledge

Students should have knowledge of:

- Computer organization: processor, memory, input/output, system bus.
- Assembly language programming: representation of data, instruction encoding, execution.
- Number systems: binary, decimal, hexadecimal.
- Programming techniques (e.g. MATLAB, C and or Python).

Course objectives

- To develop an in-depth understanding of computer systems performance.
- To be able to analyze and evaluate memory hierarchy performance.
- To understand instruction-level parallelism including pipelining and superscalar execution.
- To develop a comprehensive knowledge of thread-level parallelism, multi-core and multi-core architectures.
- To understand the main trade-offs and challenges of large-scale computers systems.

List of topics

- The Evolution of Computers
- Computer Performance
- Computer Performance
- Memory
- Instruction Level Parallelism (ILP): Pipeline
- Parallel Organization
- Instruction Level Parallelism: Superscalar
- Multicore and computer networks
- Multicore and computer networks
- System on Chip (SoC) and Embedded Microcontrollers

Learning outcomes

By the end of this course, students should be able to:

- Know the history and evolution of computer systems.
- Develop a comprehensive understanding of computer performance.
- Understand memory hierarchies in computer systems.
- Demonstrate an ability to analyze and evaluate CPU and memory hierarchy performance.
- Learn instruction-level parallelism techniques including pipelining and superscalar execution.
- Know thread-level parallelism, multi-core and many-core architectures.
- Understand computer trade-offs and challenges in complicated systems such as heterogeneous networks and Internet of Things.

Graduate Attributes (GAs)

The Canadian Engineering Accreditation Board requires graduates of engineering programs to possess 12 attributes at the time of graduation. There are no GA's related to this course. For more information, please visit: <https://engineerscanada.ca/>.

Accreditation Units (AUs)

For more information about Accreditation Units, please visit: <https://engineerscanada.ca/>.

The course has a total of 44 AUs, divided into:

- Engineering Science: 50%
- Engineering Design: 50%

Instructor and TA contact

Specific to course offering (tbd)

Textbook (or other resources)

Specific to course offering (tbd)

Evaluation and grading scheme

Specific to course offering (tbd)

Breakdown of course requirements

Specific to course offering (tbd)

Tentative week-by-week breakdown

Specific to course offering (tbd)

General regulations

Specific to course offering (tbd)